Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended): A method of fabricating an integrated circuit, the method comprising:

depositing a reflective metal material layer over a layer of polysilicon;

depositing an anti-reflective coating over the reflective metal material layer;

etching the anti-reflective coating;

trim etching the reflective metal material layer to form a mask pattern, wherein the anti-reflective coating is removed during the trim etching ; and

removing portions of the polysilicon layer using the formed mask pattern, wherein a remaining portion of the polysilicon layer is a gate structure.

2. (Previously Presented): The method of claim 1, further comprising depositing a resist layer over the anti-reflective coating.

3. (Original): The method of claim 1, wherein the step of removing portions of the anti-reflective coating comprises providing an isotropic etch to the anti-reflective coating.

4. (Original): The method of claim 1, wherein the reflective metal material layer comprises tungsten.

5. (Original): The method of claim 4, wherein the reflective metal material layer has a thickness of 80-200 Angstroms.

6. (Cancelled)

7. (Currently Amended): A method of optimizing optical properties of gate patterning to control gate size in an integrated circuit fabrication process, the method comprising:

providing a reflective metal layer over a gate material layer;

providing a mask layer over the reflective metal layer; and

patterning the gate material layer including selectively etching the mask layer, trim etching the reflective metal layer, and removing portions of the gate material layer using the trim etched reflective metal layer as a hardmask, wherein the mask layer is stripped during the trim etching of the reflective metal layer.

8. (Original): The method of claim 7, wherein the reflective metal layer comprises tungsten (W).

9. (Original): The method of claim 7, wherein the patterning step comprises trim etching the mask layer.

10. (Original): The method of claim 7, wherein the reflective metal layer has a thickness of 80-200 Angstroms.

11. (Original): The method of claim 7, wherein the step of providing a mask layer comprises depositing a layer of SiON and a layer of resist.

12. (Previously Presented): The method of claim 7, wherein the reflective metal layer is optically opaque to the gate material layer.

13. (Original): The method of claim 7, wherein the step of providing a reflective metal layer comprises selecting the reflective metal layer based on etch chemistry of the reflective metal layer and the gate material layer.

14. (Currently Amended): A method of forming a gate in an integrated circuit, the method comprising:

providing a gate material layer;

providing a reflective metal layer over the gate material layer;

providing an anti-reflective coating (ARC) layer over the reflective metal layer;

providing a resist layer over the ARC layer; and

patterning a gate structure in the gate material layer by selectively removing portions of the resist layer, ARC layer, reflective layer, and gate material layer, wherein the ARC layer and portions of the reflective layer are removed using trim etching and remaining portions of the reflective layer are used as a mask to pattern the gate material layer.

15. (Previously Presented): The method of claim 14, wherein the reflective metal layer comprises tungsten (W).

16. (Previously Presented The method of claim 14, wherein the metal material layer has a thickness of approximately 100 Angstroms.

17. (Original): The method of claim 14, wherein the ARC layer comprises SiON.

18. (Original): The method of claim 14, wherein the step of selectively removing comprises trim etching the ARC layer.

19. (Original): The method of claim 18, wherein the ARC layer is SiON.

20. (Previously Presented): The method of claim 19, wherein the reflective metal layer has a thickness of between 80 and 200 Angstroms.